

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed description]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor device which comes to form polycrystal silicon resistance on a semiconductor substrate, and its manufacture technique.

[0002]

[Object of the Invention] In the driver IC for EL drive, since a very high voltage (for example, 200V) is impressed, resistance of a high proof pressure is needed with the high proof-pressure transistor. Polycrystal silicon resistance is used as resistance in this case. The B-B cross-section structure in drawing 6 is shown in the planar structure of the polycrystal silicon resistance section (the 2nd layer insulation layer 5 is removed) used for drawing 6 at such a driver IC for EL drive, and drawing 7.

[0003] On a silicon substrate 1, the polycrystal silicon resistance 3 is formed through an oxide film 2, and the 1st and 2nd layer insulation layer 4 and 5 is formed on it. Moreover, the polycrystal silicon resistance 3 and the aluminum wiring 7 are electrically connected by the contact 6. In such a configuration, the heat which occurred by the polycrystal silicon resistance 3 radiates heat from the 1st and 2nd layer insulation layer 4 and 5.

[0004] Resistance falls, a current flows and generation of heat increases so that temperature goes up, since the temperature coefficient of the polycrystal silicon resistance 3 is positive. The polycrystal silicon resistance 3 results in a breakdown by increase of this generation of heat. Therefore, the proof pressure of the polycrystal silicon resistance 3 falls by generation of heat of the polycrystal silicon resistance 3. In this case, since the calorific value per unit area will become small if the size of the polycrystal silicon resistance 3 is enlarged, although a proof pressure can be raised, chip area will become large and a cost will increase.

[0005] this invention is what took the example by the above-mentioned problem, and it aims at raising a proof pressure, without enlarging the size of polycrystal silicon resistance.

[0006]

[The means for solving a technical problem] In order to attain the above-mentioned purpose, in invention given in the claim 1 or 4, it is characterized by forming the heat sink with thermal conductivity higher than a layer insulation layer after polycrystal silicon resistance. Therefore, the heat sink with the high thermal conductivity which has arranged the heat which occurs from polycrystal silicon resistance on polycrystal silicon resistance can be made to be able to conduct, elevation of the temperature of polycrystal silicon resistance can be suppressed, and the proof pressure of polycrystal silicon resistance can be raised.

[0007] In this case, like invention given in a claim 3, if it forms directly on polycrystal silicon resistance, using a heat sink as an insulator, the thermolysis effect can be raised more. Moreover, if a heat sink is formed like invention given in a claim 4 for a long time than the width of face of polycrystal silicon resistance so that polycrystal silicon resistance may be crossed, a heat sinking plane product can be enlarged and the thermolysis effect can be raised more.

[0008] Moreover, the thermolysis structure of polycrystal silicon resistance can be formed, without needing an excessive manufacturing process like invention given in a claim 5, at the time of formation of a wiring of a semiconductor device and polycrystal silicon resistance, if the heat sink of the same material as the wiring is formed after polycrystal silicon resistance.

[0009]

[Gestalt of implementation of invention]

(The 1st enforcement gestalt) The A-A cross-section structure in drawing 1 is shown in the planar structure of the polycrystal silicon resistance section (the 2nd layer insulation layer 5 is removed) used for semiconductor devices, such as a driver IC for EL drive which starts the 1st enforcement gestalt of this invention at drawing 1, and drawing 2.

[0010] On a silicon substrate 1, the polycrystal silicon resistance 3 is formed through an oxide film 2, and the 1st and 2nd layer insulation layer (for example, the silicon oxide of a phosphorus dope, a silicon nitride film) 4 and 5 is formed on it. Moreover, the polycrystal silicon resistance 3 and the aluminum wiring 7 are electrically connected by the contact 6. Between the 1st and 2nd layer insulation layer 4 and 5, the heat sink 8 formed with aluminum with thermal conductivity higher than those layer insulation layers 4 and 5 is formed. As shown in drawing 1, this heat sink 8 is formed for a long time than the width of face of the polycrystal silicon resistance 3 so that the polycrystal silicon resistance 3 may be crossed.

[0011] By the above-mentioned configuration, the heat which occurred by the polycrystal silicon resistance 3 radiates heat from a heat sink 8 through the 1st layer insulation layer 4. in this case, since the thermal conductivity of a heat sink 8 is higher than the layer insulation layers 4 and 5, it is shown in drawing 6 and drawing 7 -- heat can be radiated conventionally more efficiently than the thing of structure, and the temperature rise of the polycrystal silicon resistance 3 can be suppressed. Moreover, by forming a heat sink 8 for a long time than the width of face of the polycrystal silicon resistance 3, the heat sinking plane product can be enlarged and the thermolysis effect can be raised.

[0012] The thermolysis effect is shown in drawing 3. This experimental result is a thing when carrying out polycrystal silicon resistance 3 in the length of 100 micrometers, and width of face of 50 micrometers, and forming a heat sink 8 in the length of 90 micrometers, the width of face of 20 micrometers, and thickness of 1.5 micrometers with aluminum. The proof pressure is carrying out enhancement of the sheet resistance of the polycrystal silicon resistance 3 in about 20 V as for any of 6.2kohm/** and 4.1kohm/**.

[0013] in addition, the material of thermal conductivity of a heat sink 8 is higher than the layer insulation layers 4 and 5 -- as long as it is, you may use other materials. Next, the manufacture technique of the above-mentioned semiconductor device is explained using drawing 4.

In order to form the CMOS transistor 100 as a semiconductor device in the [process of drawing 4 (a)] silicon substrate 1, the N well 10 and the P well 11 are formed in it, and a gate oxide film is formed in it, and the LOCOS oxide film 2 is formed in it in other fields. And the gate 12 and the polycrystal silicon resistance 3 are formed, and the source drain 13 is formed in the N well 10 and the P well 11, respectively.

[0014] [the process of drawing 4 (b)] -- after forming the 1st layer insulation layer 4, a contact hole is formed and the aluminum wiring 7 is formed in the gate 12 of CMOS transistor, the source drain 13, and the polycrystal silicon resistance 3. The heat sink 8 described above at the time of this wiring formation is also formed simultaneous with aluminum.

[0015] The 2nd layer insulation layer 5 is formed after this [[process of drawing 4 (c)]]. Thermolysis structure can be formed, using the conventional process as it is, without according to the above-mentioned manufacture technique, using a process excessive because of formation of a heat sink 8, since a heat sink 8 can be simultaneously formed at the time of formation of the aluminum wiring 7.

(The 2nd enforcement gestalt) Although the above-mentioned 1st enforcement gestalt showed what forms a heat sink 8 through the 1st layer insulation layer 4 after the polycrystal silicon resistance 3, a heat sink 8 is formed with the insulator with thermal conductivity higher than a layer insulation layer, and it may be made to form it on the polycrystal silicon resistance 3 directly.

[0016] The cross-section structure of this 2nd enforcement gestalt is shown in drawing 5 . The planar structure is the same as that of what is shown in drawing 1 . In this 2nd enforcement gestalt, in order to contact the polycrystal silicon resistance 3 directly in a heat sink 8, the thermolysis effect higher than the 1st enforcement gestalt can be acquired, and a proof pressure can be raised much more.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

MEANS

[The means for solving a technical problem] In order to attain the above-mentioned purpose, in invention given in the claim 1 or 4, it is characterized by forming the heat sink with thermal conductivity higher than a layer insulation layer after polycrystal silicon resistance. Therefore, the heat sink with the high thermal conductivity which has arranged the heat which occurs from polycrystal silicon resistance on polycrystal silicon resistance can be made to be able to conduct, elevation of the temperature of polycrystal silicon resistance can be suppressed, and the proof pressure of polycrystal silicon resistance can be raised.

[0007] In this case, like invention given in a claim 3, if it forms directly on polycrystal silicon resistance, using a heat sink as an insulator, the thermolysis effect can be raised more. Moreover, if a heat sink is formed like invention given in a claim 4 for a long time than the width of face of polycrystal silicon resistance so that polycrystal silicon resistance may be crossed, a heat sinking plane product can be enlarged and the thermolysis effect can be raised more.

[0008] Moreover, the thermolysis structure of polycrystal silicon resistance can be formed, without needing an excessive manufacturing process like invention given in a claim 5, at the time of formation of a wiring of a semiconductor device and polycrystal silicon resistance, if the heat sink of the same material as the wiring is formed after polycrystal silicon resistance.

[0009]

[Gestalt of implementation of invention]

(The 1st enforcement gestalt) The A-A cross-section structure in drawing 1 is shown in the planar structure of the polycrystal silicon resistance section (the 2nd layer insulation layer 5 is removed) used for semiconductor devices, such as a driver IC for EL drive which starts the 1st enforcement gestalt of this invention at drawing 1, and drawing 2.

[0010] On a silicon substrate 1, the polycrystal silicon resistance 3 is formed through an oxide film 2, and the 1st and 2nd layer insulation layer (for example, the silicon oxide of a phosphorus dope, a silicon nitride film) 4 and 5 is formed on it. Moreover, the polycrystal silicon resistance 3 and the aluminum wiring 7 are electrically connected by the contact 6. Between the 1st and 2nd layer insulation layer 4 and 5, the heat sink 8 formed with aluminum with thermal conductivity higher than those layer insulation layers 4 and 5 is formed. As shown in drawing 1, this heat sink 8 is formed for a long time than the width of face of the polycrystal silicon resistance 3 so that the polycrystal silicon resistance 3 may be crossed.

[0011] By the above-mentioned configuration, the heat which occurred by the polycrystal silicon resistance 3 radiates heat from a heat sink 8 through the 1st layer insulation layer 4. In this case, since the thermal conductivity of a heat sink 8 is higher than the layer insulation layers 4 and 5, it is shown in drawing 6 and drawing 7 -- heat can be radiated conventionally more efficiently than the thing of structure, and the temperature rise of the polycrystal silicon resistance 3 can be suppressed. Moreover, by forming a heat sink 8 for a long time than the width of face of the polycrystal silicon resistance 3, the heat sinking plane product can be enlarged and the thermolysis effect can be raised.

[0012] The thermolysis effect is shown in drawing 3. This experimental result is a thing when carrying

out polycrystal silicon resistance 3 in the length of 100 micrometers, and width of face of 50 micrometers, and forming a heat sink 8 in the length of 90 micrometers, the width of face of 20 micrometers, and thickness of 1.5 micrometers with aluminum. The proof pressure is carrying out enhancement of the sheet resistance of the polycrystal silicon resistance 3 in about 20 V as for any of 6.2kohm/** and 4.1kohm/**.

[0013] in addition, the material of thermal conductivity of a heat sink 8 is higher than the layer insulation layers 4 and 5 -- as long as it is, you may use other materials Next, the manufacture technique of the above-mentioned semiconductor device is explained using drawing 4 .

In order to form the CMOS transistor 100 as a semiconductor device in the [process of drawing 4 (a)] silicon substrate 1, the N well 10 and the P well 11 are formed in it, and a gate oxide film is formed in it, and the LOCOS oxide film 2 is formed in it in other fields. And the gate 12 and the polycrystal silicon resistance 3 are formed, and the source drain 13 is formed in the N well 10 and the P well 11, respectively.

[0014] [the process of drawing 4 (b)] -- after forming the 1st layer insulation layer 4, a contact hole is formed and the aluminum wiring 7 is formed in the gate 12 of CMOS transistor, the source drain 13, and the polycrystal silicon resistance 3 The heat sink 8 described above at the time of this wiring formation is also formed simultaneous with aluminum.

[0015] The 2nd layer insulation layer 5 is formed after this [[process of drawing 4 (c)]]. Thermolysis structure can be formed, using the conventional process as it is, without according to the above-mentioned manufacture technique, using a process excessive because of formation of a heat sink 8, since a heat sink 8 can be simultaneously formed at the time of formation of the aluminum wiring 7.

(The 2nd enforcement gestalt) Although the above-mentioned 1st enforcement gestalt showed what forms a heat sink 8 through the 1st layer insulation layer 4 after the polycrystal silicon resistance 3, a heat sink 8 is formed with the insulator with thermal conductivity higher than a layer insulation layer, and it may be made to form it on the polycrystal silicon resistance 3 directly.

[0016] The cross-section structure of this 2nd enforcement gestalt is shown in drawing 5 . The planar structure is the same as that of what is shown in drawing 1 . In this 2nd enforcement gestalt, in order to contact the polycrystal silicon resistance 3 directly in a heat sink 8, the thermolysis effect higher than the 1st enforcement gestalt can be acquired, and a proof pressure can be raised much more.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim]

[Claim 1] The semiconductor device characterized by forming the heat sink (8) with thermal conductivity higher than the aforementioned layer insulation layer (4, 5) after the aforementioned polycrystal silicon resistance (3) in the semiconductor device with which polycrystal silicon resistance (3) is formed on a semiconductor substrate (1), and it comes to form a layer insulation layer (4, 5) on it.

[Claim 2] The 1st layer insulation layer with which the aforementioned layer insulation layer was formed on the aforementioned polycrystal silicon resistance (3) (4), It is a semiconductor device given in the claim 1 which consists of the 2nd layer insulation layer (5) formed on this 1st layer insulation layer, and is characterized by forming the aforementioned heat sink (8) between the layer insulation layer (4) of the above 1st, and the layer insulation layer (5) of the above 2nd.

[Claim 3] The aforementioned heat sink (8) is a semiconductor device given in the claim 1 characterized by being an insulator, being directly formed on the aforementioned polycrystal silicon resistance (3), and forming the aforementioned layer insulation layer (5) on this heat sink (8).

[Claim 4] The aforementioned heat sink (8) is the claim 1 characterized by being formed for a long time than the width of face of the aforementioned polycrystal silicon resistance (3) so that the aforementioned polycrystal silicon resistance (3) may be crossed, or the semiconductor device of any one publication of three.

[Claim 5] A semiconductor device (100) and polycrystal silicon resistance (3) are formed in a semiconductor substrate (1). In the manufacture technique of the semiconductor device which comes to form a wiring (7) of the aforementioned semiconductor device (100) and the aforementioned polycrystal silicon resistance (3) after forming a layer insulation layer (4) The manufacture technique of the semiconductor device characterized by forming the heat sink (8) of the same material as the aforementioned wiring (7) after the aforementioned polycrystal silicon resistance (3) at the time of formation of the aforementioned wiring (7).

[Translation done.]